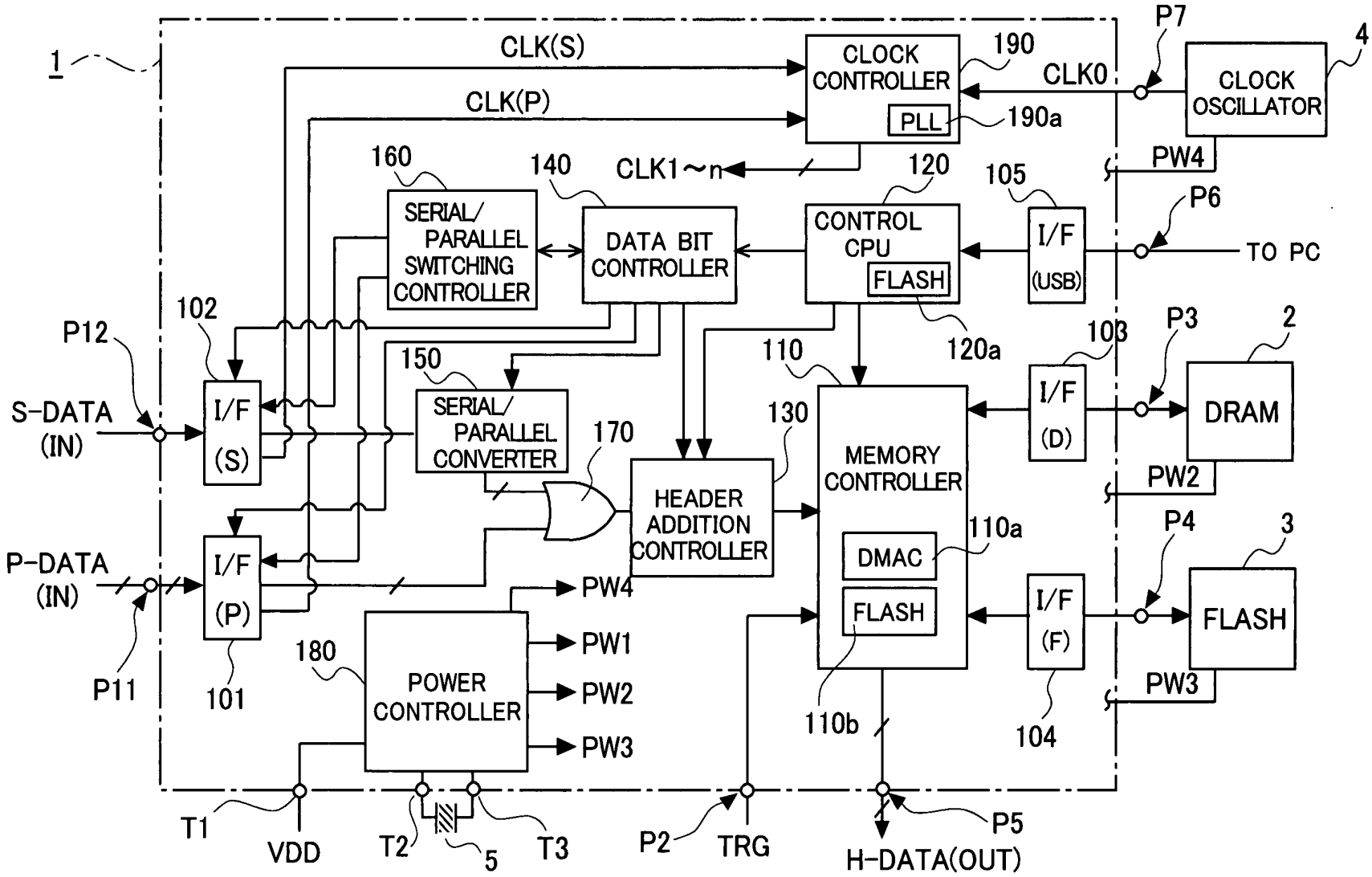
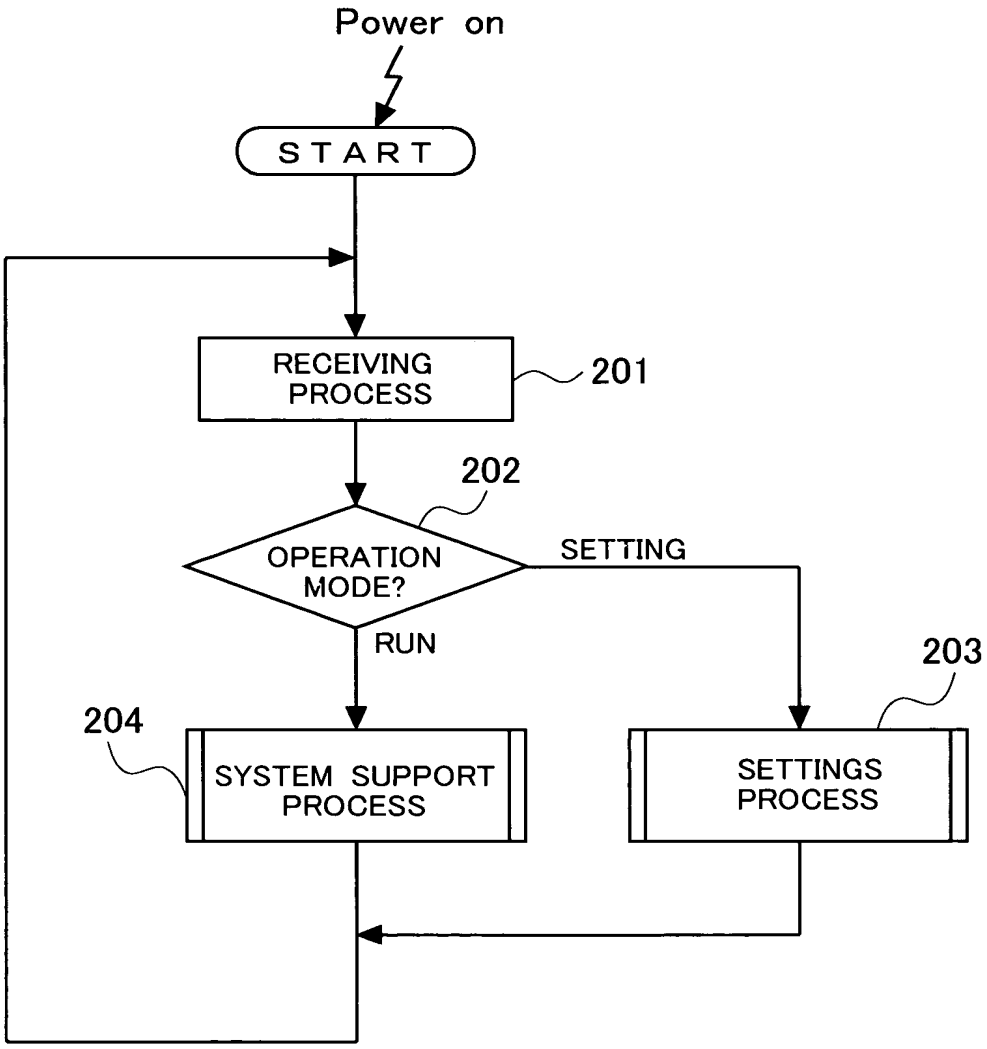
Fig. 1



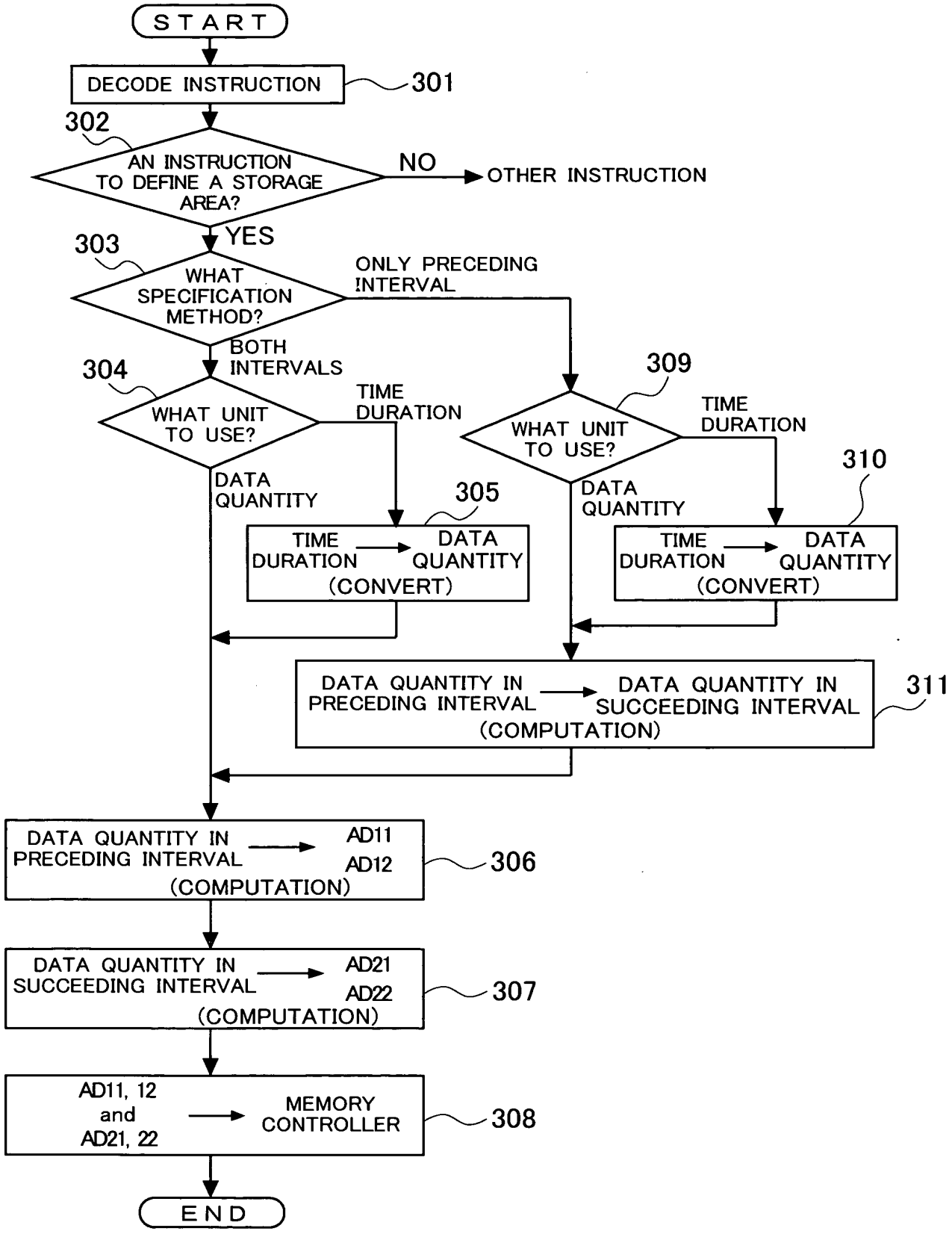
BLOCK DIAGRAM OF SAMPLE-AND-HOLD APPARATUS ACCORDING TO THE PRESENT INVENTION

Fig.2



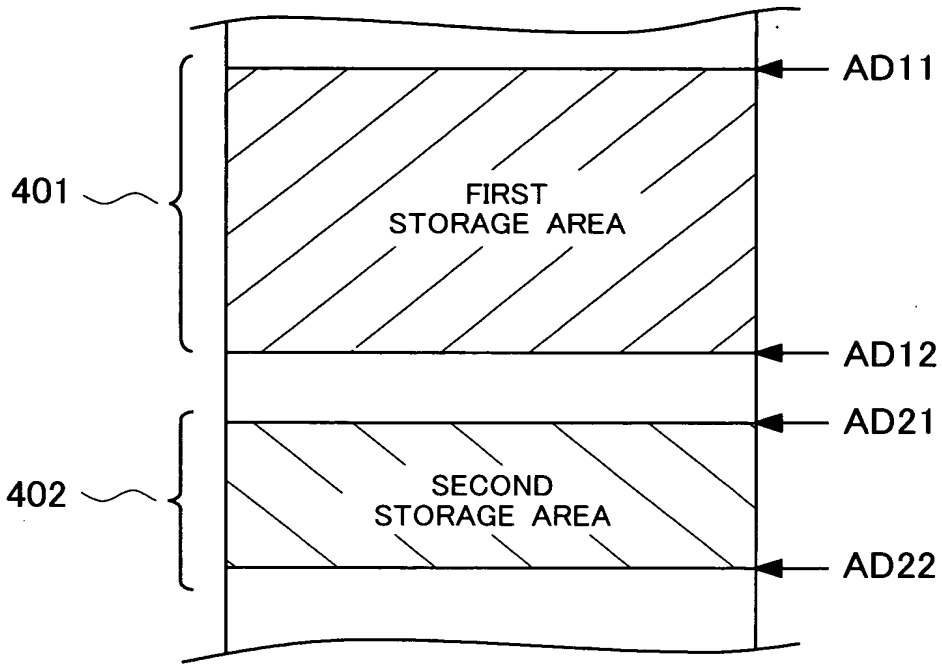
GENERAL FLOWCHART SHOWING OPERATION OF CONTROL CPU

Fig.3

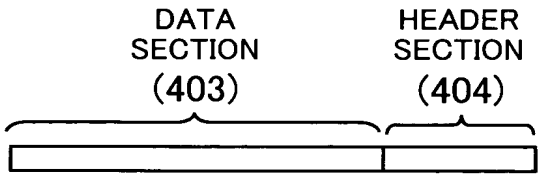


DETAILED FLOWCHART OF SETTINGS PROCESS

Fig.4



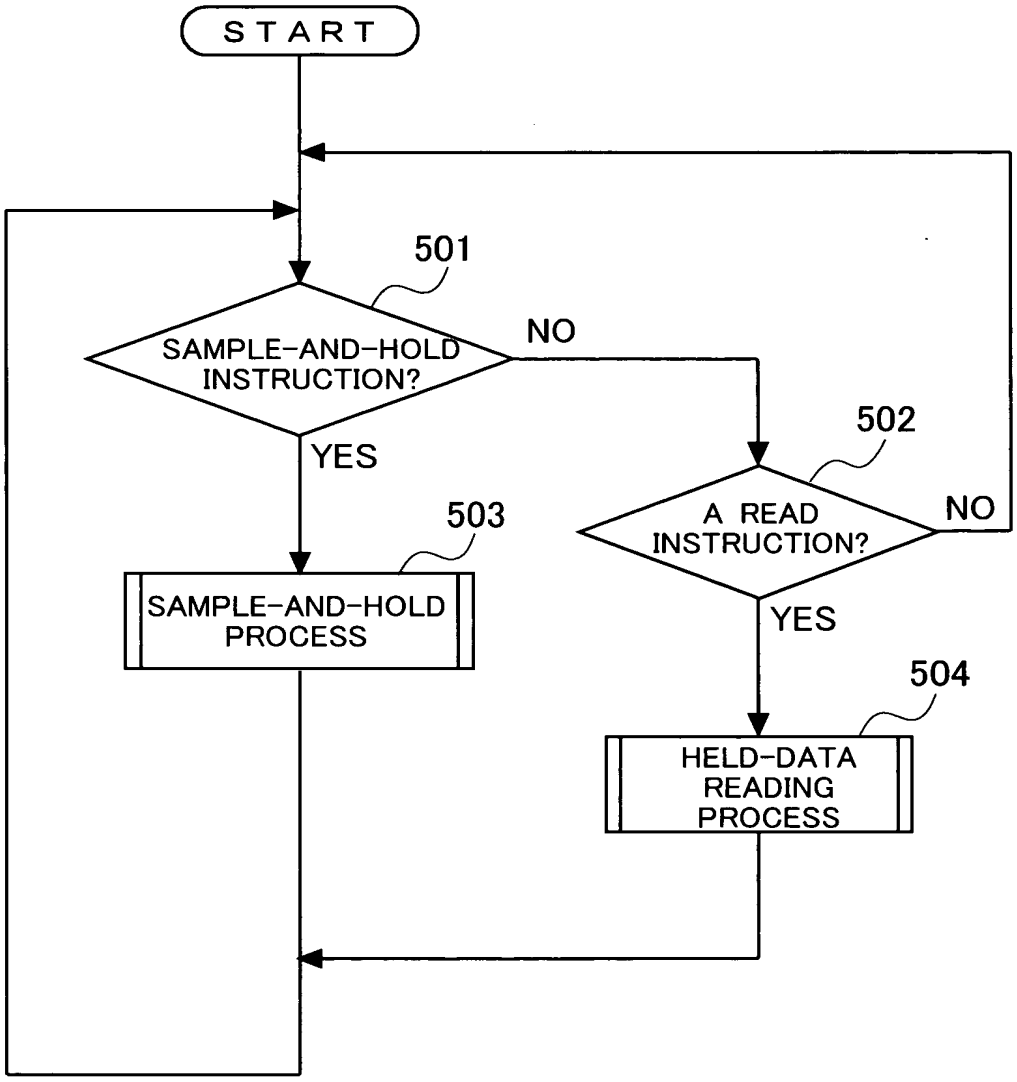
(a)



(b)

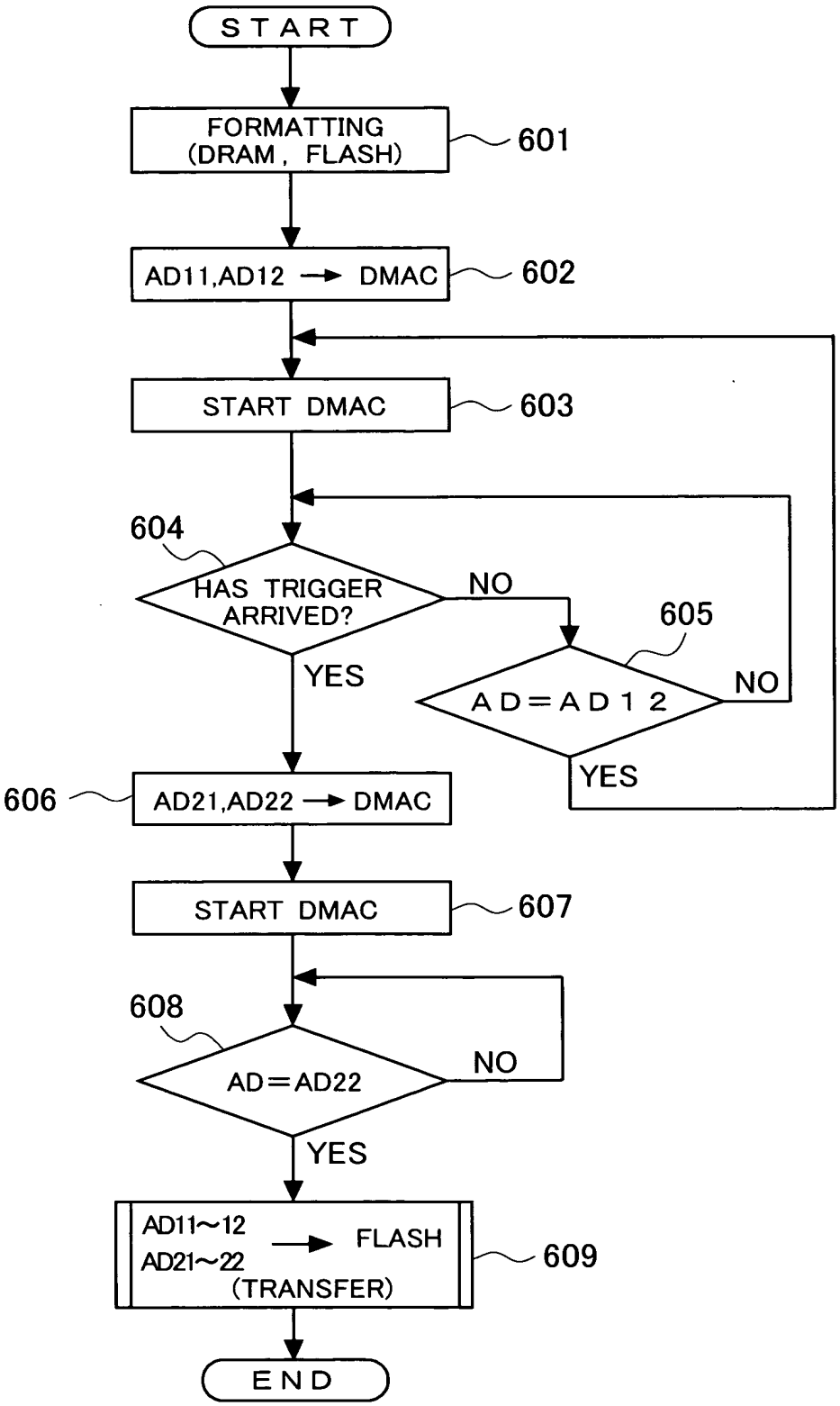
EXPLANATORY DIAGRAM ILLUSTRATING MEMORY MAP
OF PRIMARY STORAGE MEDIUM AND FORMAT OF STORED DATA

Fig.5



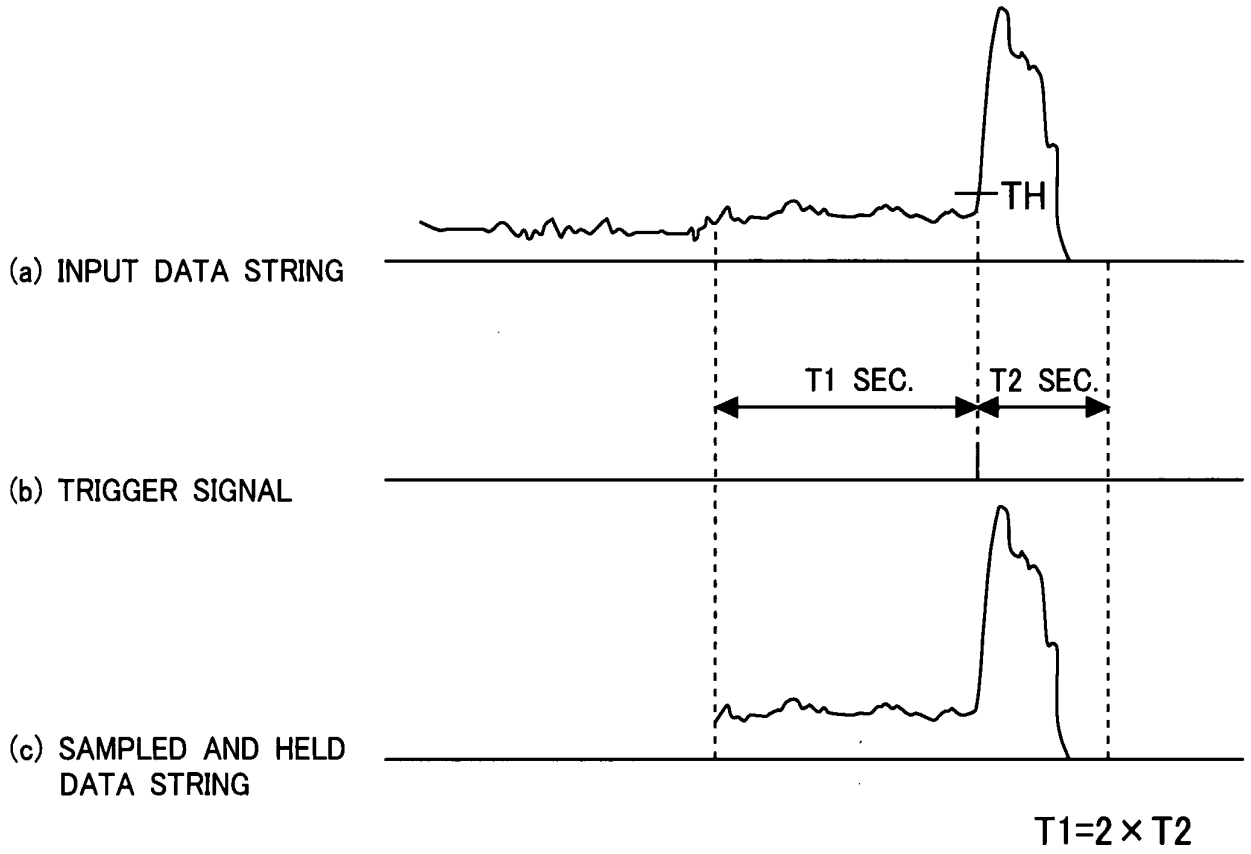
GENERAL FLOWCHART
SHOWING OPERATION OF MEMORY CONTROLLER

Fig.6



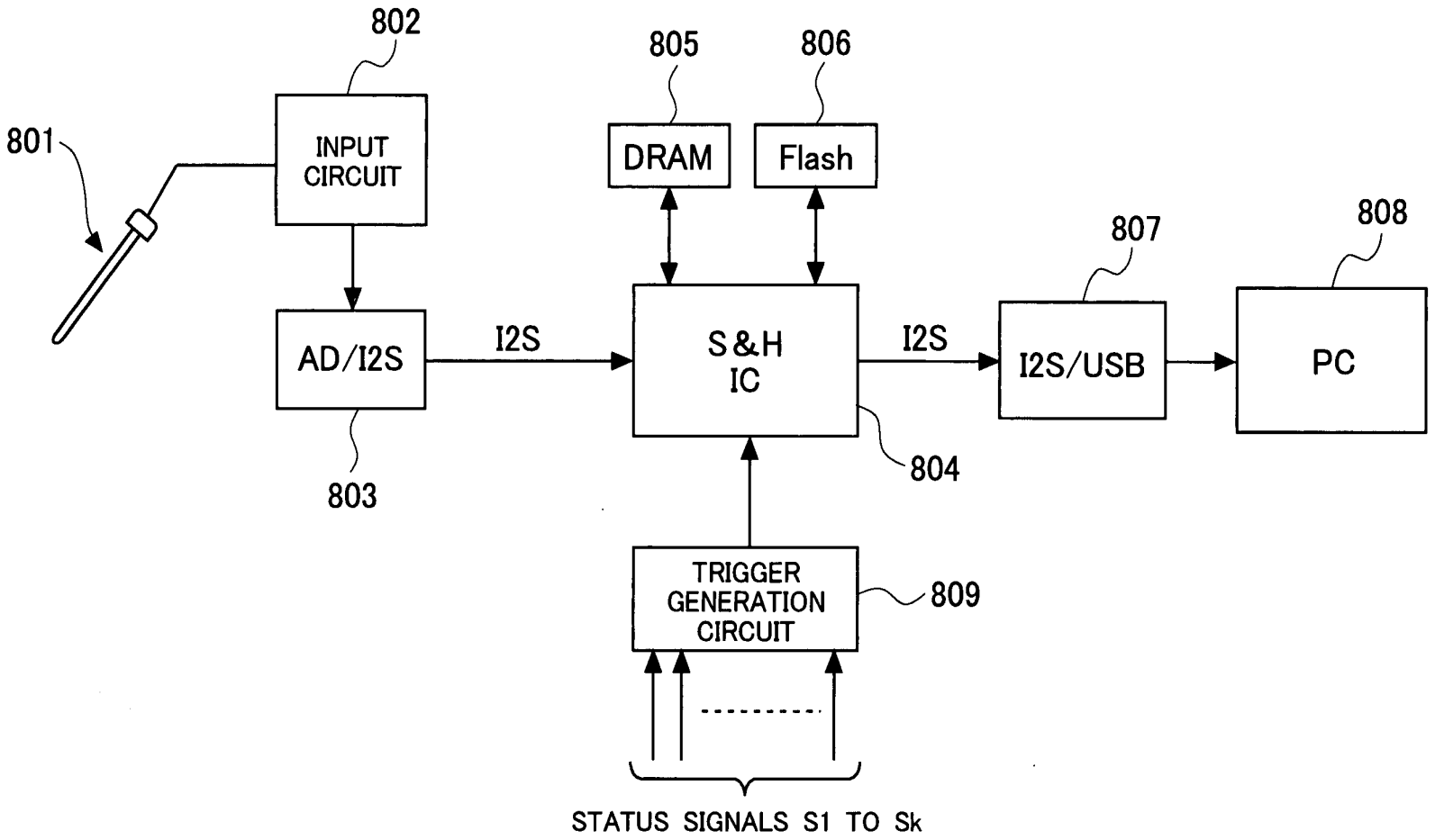
DETAILED FLOWCHART OF SAMPLE-AND-HOLD PROCESS

Fig.7



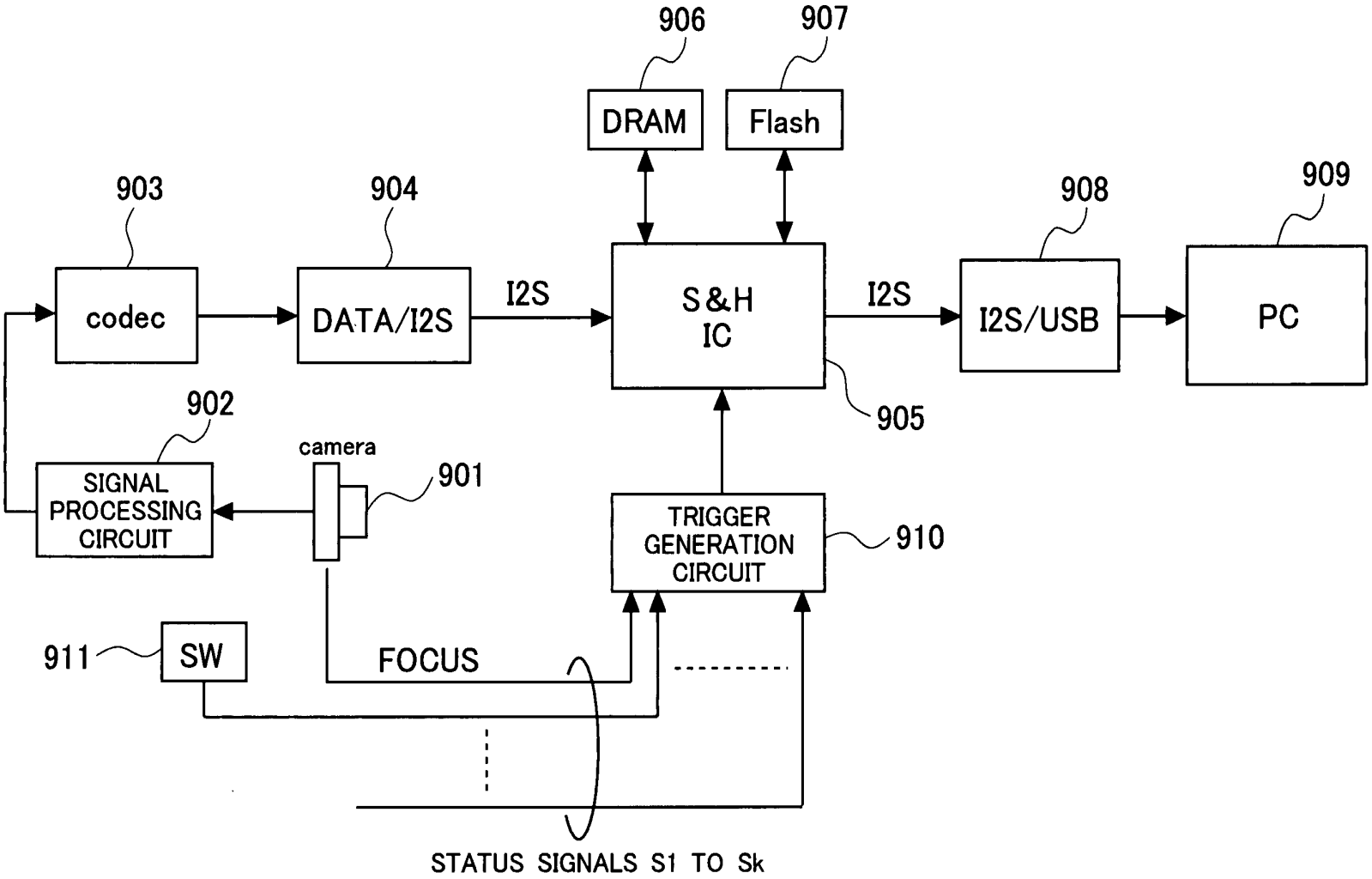
EXPLANATORY DIAGRAM ILLUSTRATING OPERATION OF THE PRESENT INVENTION

Fig.8



BLOCK DIAGRAM OF DATA RECORDER
TO WHICH IC ACCORDING TO THE PRESENT INVENTION IS APPLIED

Fig.9



BLOCK DIAGRAM OF MONITORING DEVICE
TO WHICH IC ACCORDING TO THE PRESENT INVENTION IS APPLIED